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Enhanced Device Performance of Germanium Nanowire Junctionless (GeNW-JL) MOSFETs by Germanide Contact Formation with Ar Plasma Treatment

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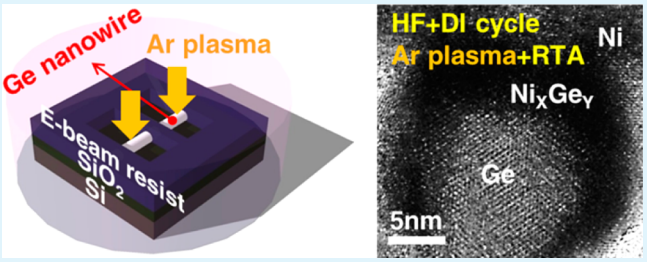
Supporting Information

ABSTRACT: In this study, germanium nanowire junctionless (GeNW-JL) metal-oxide-semiconductor-field-effect-transistors (MOSFETs) exhibited enhanced electrical performance with low source/drain (S/D) contact resistance under the influence of Ar plasma treatment on the contact regions. We found that the transformation of the surface oxide states by Ar plasma treatment affected the S/D contact resistance. With Ar plasma treatment, the germanium dioxide on the GeNW surface was effectively removed and increased oxygen vacancies were formed in the suboxide on the GeNW, whose germanium-enrichment surface was obtained to form a germanide contact at low temperature. After a rapid thermal annealing process, Ni-germanide contacts were formed on the Ar-plasma-treated GeNW surface. Ni-germanide contact resistance was improved by more than an order of magnitude compared to that of the other devices without Ni-germanide contact. Moreover, the peak field effect mobility value of the GeNW-JL MOSFETs was dramatically improved from 15 $cm^2/(V\,s)$ to 550 $cm^2/(V\,s)$, and the $I_{on/off}$ ratio was enhanced from 1×10 to 3×10^3 due to Ar plasma treatment. The Ar plasma treatment process is essential for forming uniform Ni-germanide-contacts with reduced time and low temperature. It is also crucial for increasing mass productivity and lowering the thermal budget without sacrificing the performance of GeNW-JL MOSFETs.



KEYWORDS: *GeNW-JL, MOSFETs, Ar plasma treatment, GeO_2, suboxide, germanide contact*

INTRODUCTION

Germanium is a promising semiconductor material suitable for switching devices of integrated logic circuitry because of its high intrinsic mobility and compatibility for integration on Si complementary-metal-oxide-semiconductor (CMOS) technology. Various groups have recently investigated germanium electronics in efforts to realize devices with low voltage operation and high performance characteristics by source/drain (S/D) contact engineering[1] and interface passivation[2] between a semiconductor and gate insulator. As CMOS devices are being scaled down to match the sub-20 nm design rule, ultra-shallow and abrupt junction formation is essential for reducing short channel effects (SCEs).[3] Junction formation within this nanometer scale raises a degree of difficulty in the integration process and machining for the fabrication of high performance systems.

Recently, as one of the solutions to the issues related to junction technology, junctionless metal-oxide-semiconductor field-effect transistors (MOSFETs) were proposed and demonstrated based on a silicon-on-insulator (SOI) wafer for the first time.[4,5] Their desirable characteristics include a simple fabrication process,[5,6] low junction leakage,[5] bulk conduction,[7] a low transverse electric field,[4,7] and immunity to short channel effects (SCE).[4,6] However, S/D resistance degradation is the most critical problem of junctionless MOSFETs, without additional implantation on the S/D region.[8]

A cleaning process is conventionally a critical step in semiconductor manufacturing.[9] In particular, surface preparation of germanium before depositing the S/D metal onto contact holes is imperative for the purpose of removing the native oxide formed in the air ambient and chemisorption of water molecules.[10−12] Different groups have investigated various surface preparation methods conducted prior to epitaxial growth

Received: September 16, 2013
Accepted: February 19, 2014
Published: February 19, 2014

   dx.doi.org/10.1021/am403971x | ACS Appl. Mater. Interfaces 2014, 6, 3150−3155

on the germanium substrate to make a clean and adhesive surface.[9,13,14] In particular, wet cleaning processes have been widely employed to remove the surface oxide, using halogen acid solutions such as diluted HF, HCl, HBr, and HI in Si technology.[15−17] However, in the case of germanium, a suboxide (GeO_x, $x < 2$) remains even after pretreatment using a chemical solution, because oxidants contained in the solution cannot oxidize GeO_x sufficiently to convert it into water-soluble GeO_2.[10,18]

At roughly 400 °C above the desorption temperature, an annealing method to remove the GeO_x from the germanium surface consumes the germanium by growing GeO_2 at the interface.[10,19,20] During the annealing process, desorption of GeO (g) also occurs and this can degrade the electrical properties.[21,22] It is thus necessary to develop a new technique to remove the surface oxide without consuming the germanium at low temperature to avoid the reaction mentioned above. To make high-performance GeNW-MOSFETs, surface treatment on the contact region of the oxidized germanium nanowire is essential, but very few studies have been done regarding its influence on electrical characteristics. Ar plasma treatment and its influences on electrical characteristics has not yet been reported.

In this work, germanium nanowire-based JL MOSFETs were compared to previously reported germanium plate-based JL MOSFETs[23] using a germanium-on-insulator (Ge−OI) wafer. Our devices exhibited improved performance compared to those reported in the literature.[23] By Ar plasma treatment, a cleaned and reactive germanium surface was obtained to form germanide-contacts at low temperature. Germanide-contacts reduced the contact resistance and enhanced the current drivability at low voltage.

EXPERIMENTAL PROCEDURE

We synthesized single-crystal germanium nanowires by the vapor-liquid-solid (VLS) method[24−26] using Au catalytic particles as a seed material. Au colloidal nanoparticles of 20 nm diameter were dispersed on SiO_2/Si (100), and were loaded in a chemical-vapor-deposition (CVD) chamber. For an intrinsic single-crystalline germanium nanowire, premixed germane gas in H_2 (GeH_4:H_2 = 1:10) was used as a precursor and nanowire growth was conducted under working pressure of 300 Torr and temperature of 310 °C for 5 min. For in situ p-type doping of germanium nanowire, premixed diborane gas (B_2H_6) in H_2 was subsequently injected to the same chamber and doped under working pressure of 10 Torr and temperature of 250 °C for 3 min.

One-hundred-nanometer-thick thermal oxide was grown on a heavily doped n-type silicon substrate as the bottom gate structure of junctionless MOSFETs, and the oxide at the bottom side of the wafer was removed by application of diluted hydrofluoric acid (HF:DI = 1:30) for 12 min followed by conventional cleaning. The top side of the grown thermal oxide acts as a gate insulator of the junctionless MOSFETs. To prepare Cr/Au pad metal deposited by an evaporator, we conducted photolithography and a lift-off process. Samples with the grown germanium nanowires were mixed with an IPA solution and agitated by an ultrasonic system to separate the germanium nanowires from the starting substrate. The germanium nanowires separated from the substrate were dispersed onto the top of a SiO_2/Si substrate. To make S/D contacts with Ni/Au (20 nm/70 nm) deposited by an evaporator, we carried out e-beam lithography and a lift-off process. After the e-beam photoresist was patterned, the following cleaning process steps were carried out. First, the sample was dipped into diluted hydrofluoric acid (HF:DI = 1:50) and into a deionized water (DI) solution three times respectively for 1 min. Second, Ar plasma treatment was performed by an inductively-coupled-plasma (ICP) system to introduce ion bombardment onto the Ge-NW surface under a working pressure below 1 mTorr. Ar-treated samples were exposed in the air within 10 s and subsequently shifted to the vacuum chamber of the evaporator. After Ni/Au deposition, a thermal annealing process was executed in a rapid thermal annealing (RTA) system under 320 °C for 30 s.

RESULTS AND DISCUSSION

Figure 1a shows a scanning-electron-microscope (SEM) image of GeNWs grown by CVD at 310 °C on a SiO_2/Si substrate.

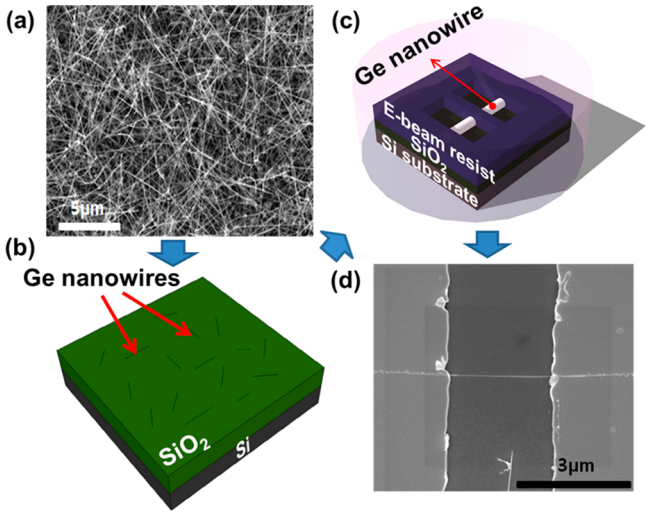


Figure 1. (a) SEM image of germanium nanowire grown by CVD on the SiO_2/Si. (b) Schematic diagram of the dispersed GeNW on SiO_2/Si substrate. (c) Schematic diagram of S/D patterned with e-beam resist by e-beam lithography. Opened S/D area was processed with various surface treatments: (I) reference sample, (II) HF+DI cycle sample, (III) Ar plasma treatment sample, (IV) HF+DI cycle+Ar plasma treatment sample. (d) Top view of SEM image of fabricated p-type Ge-NW JL MOSFET.

Figure 1b shows a schematic diagram of the dispersed germanium nanowires on SiO_2/Si substrate. Figure 1c shows a schematic diagram of S/D patterned with e-beam resist by e-beam lithography. The opened S/D region was processed with various surface treatments ((I) reference sample, (II) HF+DI cycle sample, (III) Ar plasma treatment sample, (IV) HF+DI cycle+Ar plasma treatment sample). Figure 1d shows the top view of a SEM image of a fabricated p-type GeNW-JL MOSFET. The intensity with respect to the binding energy was inspected by a X-ray Photoelectron Spectroscopy (XPS) system (Thermo Scientific, model MultiLab 2000) having a spherical sector analyzer and aluminum Kα line with a photon energy of 1486.6 eV. All samples were loaded in an ultrahigh vacuum (UHV) of 5 x 10^{-10} mbar. Ge nanowires grown on a SiO_2/Si substrate were used as samples for XPS analyses, and these samples were investigated to confirm the effects of surface treatment such as wet HF+DI cycle and dry Ar plasma treatment processes. XPS spectra of the surface treated samples are shown in Figure 3 and Figure S1 in the Supporting Information, and the percentage ratio of the germanium and various germanium oxides are tabulated in Table S1 and Table S2 in the Supporting Information. Deconvoluted peaks are summarized in Figure 2 and Figure S2 in the Supporting Information. We have used the carbon peak (C1s = 285.4 eV) to calibrate all samples with a reference sample. To extract the peak areas of the germanium and various germanium oxides, XPS spectra were deconvoluted into five peak lines to fit the Ge3d spectra, corresponding to Ge (Ge^0), Ge_2O (Ge^{1+}), GeO (Ge^{2+}), Ge_2O_3 (Ge^{3+}), and GeO_2 (Ge^{4+}).[27−29] The main peak of Ge3d appeared at 29.7 eV, which

dx.doi.org/10.1021/am403971x | ACS Appl. Mater. Interfaces 2014, 6, 3150−3155

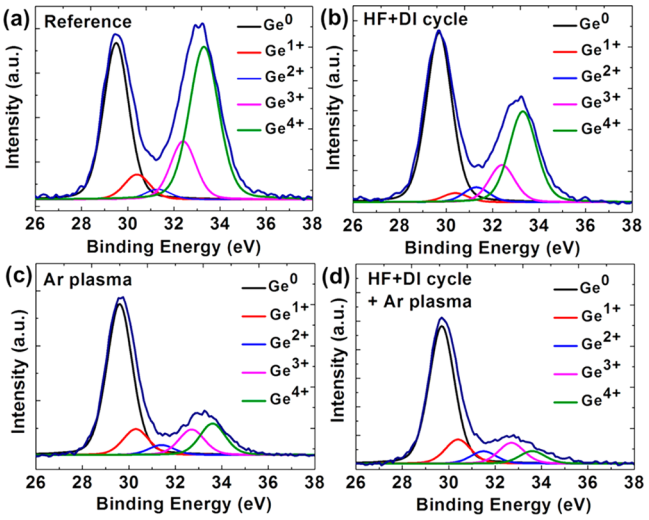


Figure 2. Ge3d peak spectra of the germanium and germanium oxides in various surface treatment conditions. (a) Reference sample (as-grown sample, air-exposed without any surface treatment), (b) HF+DI cycle sample, (c) Ar plasma treatment sample, (d) HF+DI cycle + Ar plasma treatment sample.

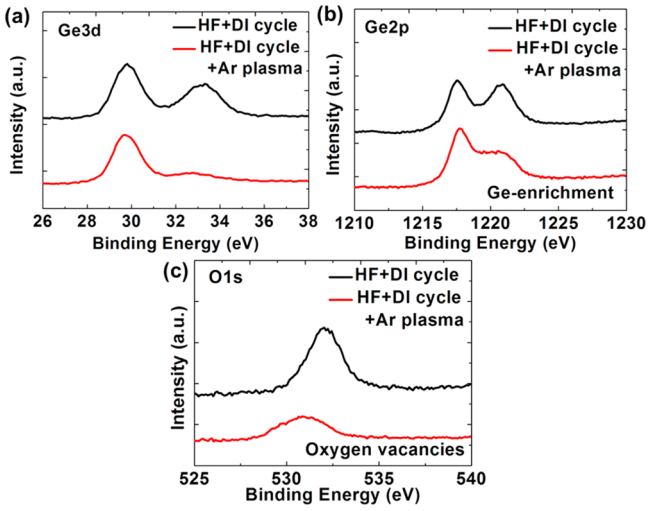


Figure 3. (a) Ge3d core-level spectra without and with Ar plasma treatment. (b) Ge2p core-level spectra without and with Ar plasma treatment. (c) O1s core-level spectra without and with Ar plasma treatment.

is related to Ge^0, and the core-level shifts of the various oxidation states levels were consistent with those in the literature reported for a Ge wafer.[29] The full width at half maxima (FWHMs) of all samples were fixed at a value of 1.4 eV, and the fitting method of all samples was based on a combination of Gaussian and Lorentzian with a ratio of 7:3.[29]

To investigate the oxide removal effect of our surface treatment methods, we started with a reference sample having 41.3 percent (%) GeO_2 on the nanowire surface, which was confirmed by deconvolution of the XPS spectra, as shown in Table S1 in the Supporting Information. Figure 2a shows that the GeO_2 (Ge^{4+}) peak intensity of the reference sample (as-grown sample, air-exposed without any surface treatment) is higher than the summation of the germanium suboxides (Ge^{1+}, Ge^{2+}, and Ge^{3+}) intensity, indicating that germanium nanowires of reference sample were dominantly encapsulated with germanium dioxide. GeO_2 peak of the sample treated with HF+DI cycle is lower than that of the reference sample and the difference in the germanium suboxide (Ge^{1+}, Ge^{2+}, and Ge^{3+}) summation is below 3 % (see Table S1 in the Supporting Information). This indicates that GeO_2 was etched during the HF+DI cycle treatment because of properties of the germanium oxide, which reacted with fluoride and the aqueous solution.[10,15]

As shown in Figure 3a, with Ar plasma treatment, GeO_2 was reduced by more than 15% and the suboxide summation was increased by more than 9% compared to the HF+DI cycle sample. This indicates that Ar plasma treatment breaks bonds in GeO_2, changing compositions toward suboxides. The composition-altered surface layer of the Ar treated sample was thus dominantly composed of suboxide such as Ge_2O_3 and Ge_2O after removing the GeO_2. Peak broadening of the oxide component is clearly shown in Figure 3b and this is ascribed to the higher surface sensitivity of the Ge2p electrons.[18]

As shown in Figure 3c, higher oxidation states were removed and lower oxidation states were formed at the nanowire surface by Ar ion bombardment, as confirmed by peak broadening and a chemical shift to the lower binding energy side in the XPS spectra. The atomic percentage of oxygen in the Ge−O bond was reduced from 60 to 45 with Ar plasma treatment (see Table S2 in the Supporting Information), indicating that oxygen deficiency is increased due to preferential sputtering of oxygen. With Ar plasma treatment only, a chemical shift occurs to the lower binding energy side, resulting in an atomic percentage reduction of oxygen in the Ge−O bond, consistent with previous results.

As shown in Table S3 in the Supporting Information, the nonstoichiometric ratio of Ge3d and O1s was due to a mixed germanium suboxide on the nanowire surface. With Ar plasma treatment, the ratio was changed to a Ge-enrichment state. As in the preceding XPS data results, Ge-enrichment occurs as shown in the EELS spectrum, which was obtained to verify the state of the interface oxide.[30−32] In the case of p-type germanium nanowire, when the oxide was completely eliminated from the nanowire surface by high-temperature thermal annealing, the $Ge^0$3d peak was shifted from 29.8 to 29.5 because of recovery of band bending at the surface between the germanium and germanium oxide.[33] However, with Ar plasma treatment, the Ge^0 peak was not shifted to lower binding energy in the Ge3d spectra.

Germanium oxide existed at the interface between the S/D metal and the germanium nanowire, which was confirmed by the peak of the localized oxygen K edge arising from O−O scattering at around 530 eV,[34] and this peak decreased as the number of O second-nearest neighbors around the excited O atoms decreased.[35] As shown in Figure 4a HRTEM image of HF+DI cycle sample, one can distinguish amorphous GeO_2 region from Ge crystalline region. The result from oxygen map image of Figure 4b was consistent with HRTEM image. But, the interface between Ni and Ge nanowire of the Ar-treated device after the HF+DI cycle was crystallized as shown in Figure 4c. This result from oxygen map image of Figure 4d was strikingly different from that of Figure 4b. EELS spectra were extracted from area region marked on panels b and d in Figure 4. As shown in Figure 4e, the difference in intensities between the nontreated sample and the Ar-treated sample at around 530 eV was due to reduced O atoms. The reduced peak, shown in Figure 4e, indicates that more O second-nearest neighbors are missing, resulting in a Ge enrichment environment.[35]

High-resolution transmission electron microscopy (HR-TEM), scanning transmission electron microscopy (STEM), and energy-dispersive spectroscopy (EDS) were conducted to

dx.doi.org/10.1021/am403971x | ACS Appl. Mater. Interfaces 2014, 6, 3150−3155

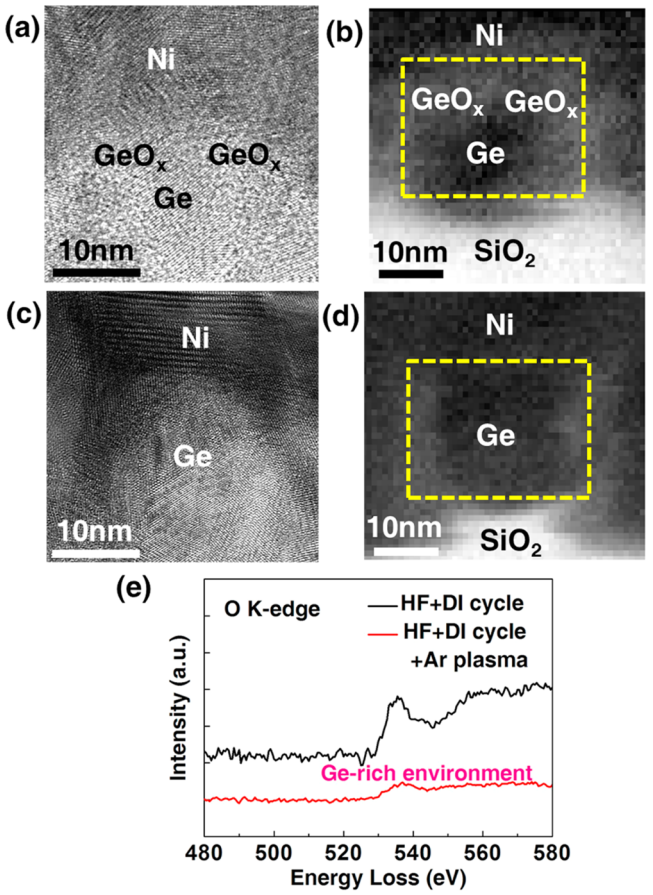


Figure 4. (a) HRTEM image of HF+DI cycle-treated device. (b) EELS oxygen map of HF+DI cycle-treated device. (c) HRTEM image of HF +DI cycle+Ar plasma-treated device. (d) EELS oxygen map of HF+DI cycle+Ar plasma-treated device. (e) EELS spectra of germanium nanowire without and with Ar plasma treatment after HF+DI cycle.

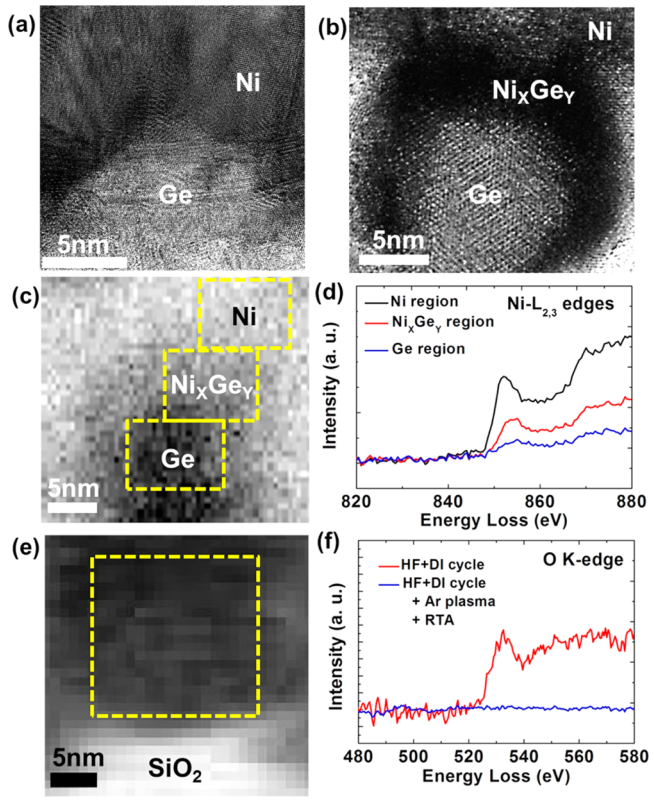


Figure 5. (a) HRTEM image of the device treated with HF+DI cycle and annealed at 320 °C (b) HRTEM image of the device treated with HF+DI cycle+Ar plasma treatment and annealed at 320 °C. (c) EELS nickel map of the device treated with HF+DI cycle+Ar plasma treatment and annealed at 320 °C. (d) EELS spectra of the device treated with HF +DI cycle+Ar plasma treatment and annealed at 320 °C with various marked region : Ni region, Ni_XGe_Y region, Ge region. (e) EELS oxygen map of the device treated with HF+DI cycle+Ar plasma treatment and annealed at 320 °C. (f) EELS spectra comparison.

verify germanide-contact formation.[36] Because GeO_x converts to GeO_2 above 400 °C, germanium will be consumed as oxide grows on the surface.[10] The thermal process conditions were thus fixed below 400 °C.

HF+DI cycle-only samples were compared to Ar-treated sample in order to study the effects of Ge enrichment of the nanowire surface on germanide contact formation after the thermal annealing process. In the HF+DI cycle sample case, as shown in Figure 5a, Ni-germinide contact was not formed at the germanium nanowire surface because of the unremoved surface oxide, which blocked the nickel diffusion. This means that, at low temperature, diffusion was retarded because of the absence of atom diffusion paths such as dislocation sites and grain boundaries.[37] However, as shown in Figure 5b, a germanide contact was successfully formed at the surface of GeNW treated with Ar plasma; this is ascribed to the high density of oxygen vacancies in the Ge enrichment environment. As shown in panels c and d in Figure 5, nickel and germanium were intermixed at the surface of nanowire, indicating that amorphous Ni_xGe_y germanide was formed at the surface of nanowire. As shown in panels e and f in Figure 5, the sample treated with HF+DI cycle +Ar plasma treatment and annealed at 320 °C has no oxygen at the interface between germanium and nickel. Diffusion of Ni-metal to germanium is much more dependent on vacancy mediation than in the case of silicon, suggesting that Ni-metal can effectively diffuse through the series of vacant cations and oxygen can diffuse out through the vacancy sites, leading to the formation of uniform Ni-germanide contact (see Figures S4 and S5 in the Supporting Information).[34] Uniform germanide contact is required to prevent saturation of the allowed density of states (DOS), which is one of the main factors limiting carrier transport in nanometer-range contact.

The performance of different GeNW-JL MOSFETs is compared to verify the effects of the Ar plasma treatment on contact resistance and device characteristics, which were measured by a semiconductor device analyzer (Agilent Technologies, model B1500). The channel length and nanowire diameters of all devices were fixed at 3 μm and 15 nm, respectively, as shown in Figures 1d and 5b. It was found that the sum of resistance $R_{CH} + R_{SD}$ is equal to 3.8 MΩ ($V_{GS} = 0$ V) after the thermal process at 320 °C. Before germanide contact formation, the resistance values were more than an order of magnitude higher compared to the Ar-treated device, as shown in Figure 6a.

In the off-state operation region ($V_{GS} = 0$ V) of junctionless MOSFETs, the channel resistance is dominant due to depleted charges in the channel region resulting from band bending at the narrow germanium channel region due to the work function difference between the channel and the gate electrode.[38] However, before annealing, the resistance R_{SD} is dominant, thereby leading to pA range current at $V_{DS} = -0.2$ V. When the channel is formed in the on-state ($V_{GS} \approx -2$ V > V_{TH}), the S/D

dx.doi.org/10.1021/am403971x | ACS Appl. Mater. Interfaces 2014, 6, 3150−3155

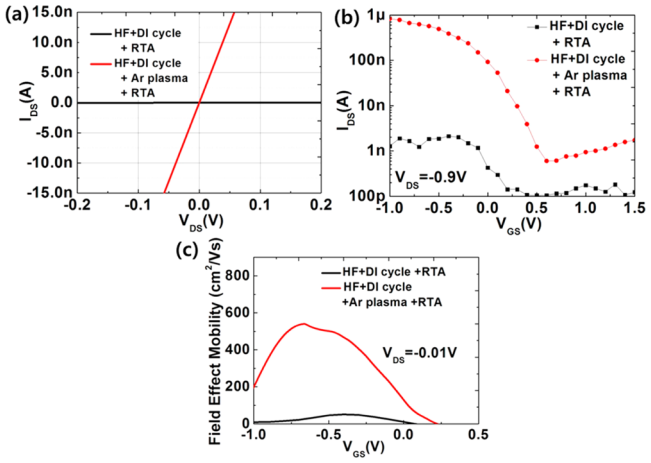


Figure 6. (a) Two-terminal electrical characteristics of the devices without and with Ar plasma treatment. (b) Transfer characteristics of the devices without and with Ar plasma treatment. (c) Field effect mobility of the devices without and with Ar plasma treatment.

contact resistance is the dominant factor limiting the carrier transport, by neglecting the channel resistance due to the highly doped channel in junctionless MOSFETs. During the on-state, the resistance $R_{CH} + R_{SD}$ was below 420 kΩ; this low value is due to recovery of depleted charges in the channel region.[5]

From the transfer characteristics shown in Figure 6b, it was found that the threshold voltage of the untreated device was higher and the on-off current ratio was lower relative to the Ar-treated device, suggesting that charge transport characteristics through the contact regions were dramatically improved by the germanide-contact due to Ar plasma treatment. Ge-NW MOSFETs exhibited a subthreshold voltage swing of 110 mV/decade, threshold voltage of a −0.2 V, and on-off current ratio of 3×10^3, and the gate leakage current was maintained below the off-state current through the whole region of device operation. The threshold voltage was extracted from constant drain current of 200 nA.

To extract the field effect mobility, the capacitance was extracted by a cylinder-on-plate model,[39] and the field effect mobility of bottom gate Ge-NW JL MOSFETs was extracted from FET characteristics reported in the literature.[39] As shown in Figure 6c, the peak of the field effect mobility in the linear operation region was 550 $cm^2/(V\ s)$. At the saturation region ($V_{DS} = -0.9$ V), the gate drivability is higher than that reported in the literature[23,40] in terms of the subthreshold voltage slope and the threshold voltage for low power operation. Ge-NW JL MOSFETs were successfully demonstrated for the first time, and the on current normalized by the diameter of the nanowire (divided by $\pi \times$ diameter) was 17 $\mu A/\mu m$, which is also higher than the values in the literature.[23,40] The p-type doping level in Ge-NW can be obtained from the relation between resistivity and mobility, corresponding to a doping level close to 4×10^{18} cm^{-3}. Output characteristics of the treated device and the resistance of the channel were well modulated by an order of magnitude (see Figure S6c in the Supporting Information).

In junctionless transistors, the difference between the gate electrode work function and the fermi level of the channel material can affect the off current characteristics of the devices and the subthreshold-voltage slope. Thus, a highly n-type doped Si wafer was used to achieve a low work function to reduce the off current and to control the threshold voltage for high quality junctionless transistor operation.[4−6] The subthreshold-voltage swing of the devices was optimized by shrinking the gate insulator thickness, and the off current was also reduced by avoiding the voltage drop across the oxide, achieving band bending of the germanium nanowires to deplete holes in the channel region.

The reason the GeNW JL MOSFETs are well-designed to deplete holes in the channel and reduce the off current, is based on a relation that can be found in the literature.[23] As a result of shrinking the oxide thickness channel length and using a multi-nanowire scheme, Ge-NW JL MOSFETs are a promising candidate for low-power and high-performance integrated logic circuits.

SUMMARY AND CONCLUSION

In summary, we demonstrated germanium nanowire-based junctionless (GeNW-JL) MOSFETs and they exhibited improved performance compared to devices without Ar plasma treatment. In addition, we investigated the effects of Ar plasma treatment on chemical properties of the germanium nanowire surface and the electrical properties of the S/D contact region. As a result of effective treatment for oxygen vacancies and a Ge enrichment environment at the surface, the contact resistance of the Ar plasma-treated device was reduced by more than an order of magnitude after thermal processing at low temperature. This achievement resulted from uniform germanidation between the nickel and germanium nanowire surface. Enhanced device performance including peak field-effect mobility of 550 $cm^2/(V\ s)$, an $I_{on/off}$ ratio of 3×10^3, a subthreshold-voltage-swing of 110 mV/decade, and enhancement mode operation with a threshold voltage of −0.2 V were thereby achieved. In conclusion, oxides such as GeO_2 and suboxides grown in the air ambient and regrown in solution can be effectively removed by Ar plasma treatment. This is a promising process because it can be carried out in a few minutes at low temperature, and it improves the S/D resistance between germanium nanowire and S/D electrodes. Our process is thus expected to be practically applied in preventing electrical characteristic degradation of GeNW-JL MOSFETs for future electronics.

ASSOCIATED CONTENT

Supporting Information

XPS spectra of Ge3d, Ge2p, and O1s in various treatment conditions. XPS peak area percentages of Ge3d and O1s in various treatment conditions. HRTEM image and FFT of cross section of reference sample. EDS maps of devices treated in various conditions. Lateral and vertical profiles of the EDS maps of device treated with HF+DI cycle+Ar plasma treatment and thermal annealing. At various V_G and V_D, transfer and output characteristics of device treated with HF+DI cycle+Ar plasma treatment and thermal annealing. This material is available free of charge via the Internet at http://pubs.acs.org/.

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Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

This work was supported by the Center for Integrated Smart Sensors funded by the Ministry of Science, ICT & Future Planning as Global Frontier Project (CISS-2012054187)

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